High Performance Computing of the
PIC Code by Using Accelerators

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The particle-in-cell (PIC) code has been revealed to be one of the most powerful tools to investigate complex and mysterious plasma phenomena. The convolutional algorithm of the PIC code assumes sequential computations. The parallel performance of the PIC code on massive-parallel-computers has been attained by the particle and/or domain decomposition algorithms using message-passing-interface (MPI) in which processes use the distributed memory system. Recent super computers tend to have accelerators such as graphics processing unit (GPU) or coprocessors using Intel Many Integrated Core Architecture (MIC). So in the lowest order of the parallel hierarchy (including multi core processor) in which each thread uses the shared memory system, it is important to use new algorithms. This study is based on the ideas of References [1,2]. The mesh parallel algorithm is used for parallelization instead of the particle parallel algorithm. In the mesh parallel algorithm each thread treat one cell (or tile consisting of several cells) and particles in the cell (tile), while each thread treats one particle in the particle parallel algorithm. Although the two major constituents of the PIC code, particle pushing and charge assignment (on the grids), are well parallelized in the mesh parallel algorithm, the additional particle redistribution after particle pushing is inevitable. The followings will be reported in the workshop.

(1) The mesh parallel oriented 2D-PIC code, basically written by using do-loops for the meshes, and its parallel performance.

(2) The acceleration of 2D-PIC code on GPU by using accelerator FORTRAN being capable of Compute Unified Device Architecture (CUDA) developed by NVIDIA.

(3) The acceleration of 2D-PIC code on Intel Phi coprocessor (HELIOS).